1.1

Foundational Technology Layers

PROCESS TECHNOLOGIES, EQUIPMENT, MATERIALS AND MANUFACTURING

1.1 PROCESS TECHNOLOGY, EQUIPMENT, MATERIALS AND MANUFACTURING

Semiconductor process technology, equipment, materials and manufacturing form the foundation of the ECS value chain producing the chip and packaged chip-level building blocks for all digital applications.

Nano- and microelectronics are key to achieving digital sovereignty in Europe, and they offer a range of solutions for a green and sustainable society. If Europe wants to control the development of a digital future fitted to its citizens and their requirements, as well as its social, economic, industrial and environmental goals, it needs continuous innovation in the field of semiconductor technology.

1.1.1 Scope

The key scope of this section is to cover all process technologies, equipment and materials' research and innovation to enable semiconductor IC manufacturing inside a cleanroom environment. This includes:

- New materials and engineered substrates to improve device performance,
- Process technologies, equipment and manufacturing technology to advance integrated circuit (IC) functionality and/or systems on chips,
- Wafer level integration addressing a technology of packaging a die while it is still on the undiced wafer or bonded/attached to a wafer (D2W). Protective layers and electrical connections are added to the substrate before dicing.

Clearly, the scope of this section as indicated in the figure below involves synergies with other sections in this ECS-SRIA. First and foremost, the section links with Components, Modules and System Integration in Chapter 1.2. In addition, this section also links with Embedded Software and System of Systems (SoS) to allow for an integral system technology co-optimisation approach to deliver application-driven solutions. More details about the synergies with other sections are described in sub-section 1.1.6.

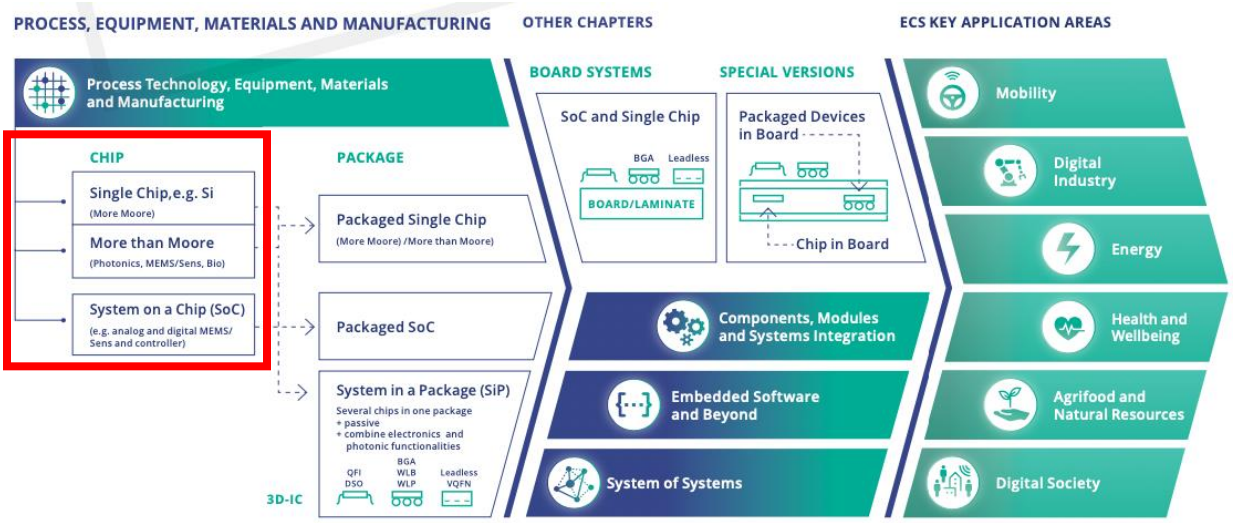

Figure 1.1.1 - The chip and packaged chip-level building blocks are the starting point for the other ECS-SRIA Chapters

1.1.2 Application breakthroughs

The main breakthrough enabled by the technological advances discussed in this section concerns the reduction of energy consumption in the various electronic components without any decrease in their performance.

In 2022, the globally consumed power of data centres alone was 240-340 TWh[1], which represents between 1-1.3% of global final electricity demand. This excludes energy used for cryptocurrency mining, which was estimated to be around 110 TWh in 2022, accounting for 0.4% of annual global electricity demand. Investing in more efficient IT hardware including microchips will provide the means to flatten this curve whilst data centre workloads are expected to dramatically increase[2].

Reducing the energy consumption of electronic components is essential for improving the autonomy of electric and hybrid vehicles, the lifetime of battery-powered sensors (for health monitoring, preserving natural resources such as water through more efficient irrigation, etc.), as well as for the development of autonomous sensors with energy harvesters and energy storage.

Since moving data from the logic cores to the adjacent memories is the main contributor to the energy consumption of logic devices (microprocessing units (MPUs), microcontroller units (MCUs), etc), their conventional von Neumann architecture must be drastically changed in close co-optimisation with other technology innovations. Near-memory or in-memory computing and neuromorphic computing are new architecture paradigms that strongly reduce the movement of data, and accordingly allow decreased overall energy consumption. Specific low- power transistors, memory and 3D-integration technologies need to be developed to ensure close coupling between computer and memory blocks.

The adoption of wide bandgap materials such as GaN and SiC is crucial for allowing higher operating temperatures and reducing the switching losses in power electronics for a broad range of power systems, such as smart phone/tablet chargers, industrial power supplies, power supplies for servers, etc., and - very important - electric vehicles, as well as to increase their range. GaN/SiC is also important for increasing the power efficiency of 5G RF base stations. In addition, GaN/Si and GaN/SOI can induce the same effect in RF front-end modules when combined with high thermally conductive materials.

The exponential increase in internet traffic (with a CAGR at 24% from 2021 to 2026[3]) sets demanding requirements on data communication technologies. New architectures and technologies will be also essential for the future development of 6G communications, for improving the bandwidth and data transmission rate, while exhibiting lower latency and lower power consumption.

Optical interconnects enable higher bandwidth- distance products, higher bandwidth density, lower electromagnetic interference, and potentially lower power consumption than electrical interconnects. They are being deployed at increasingly shorter distances – for example, within and between data centres. In the longer term, chip-to-chip and even intra-chip communication may be performed with CMOS-compatible photonics. Beyond these applications, emerging precision applications – including

[1] https://www.iea.org/energy-system/buildings/data-centres-and-data-transmission-networks
[2] https://www.iea.org/commentaries/data-centres-and-energy-from-global-headlines-to-local-headaches
[3] https://blog.gitnux.com/internet-traffic-statistics/

atomic clocks, precision metrology, and transformative applications such as quantum communications and information processing – will also benefit from photonic capabilities integrated with electronics. These photonic capabilities range from silicon and heterogeneous III/V (membrane) photonics, to potentially disruptive technologies such as nanophotonics, and 2-D materials or graphene-based photonics. Additionally, developments in novel computing paradigms such as photonic and quantum computing threaten to make current security protocols insecure and will require the development of novel, future-proof cryptographic methods.

Other breakthroughs will concern adding intelligence close to the sensors (Intelligence at the edge) and/or to the data sources (IoT), and to integrate the components in a form factor that perfectly suits their applications. The initial generation of "Internet-of-Things" management was cloud-centric, where sensor data were collected from the periphery (or "edge"), then processed and analysed at the enterprise or platform tier. However, in that case, a tremendous amount of data needs to flow to the cloud and back, and a large amount of data processing power is required to structure and analyse it. In such a cloud-focused solution, latency and privacy concerns are often worrisome, or even prohibitive.

The term "embedded AI" or "edge AI" denotes how AI algorithms can be processed locally on a hardware device (e.g. a sensor) close to where the data is generated, and an action may then be required. A device using edge AI can process data it has collected and subsequently take decisions independently, without connecting to a central processing unit (CPU). Where initially local decisions will be supported by inference actions, there will be an evolution to training on the edge devices. Edge AI extends embedded computing, and contributes to economically effective solutions for the societal challenges we are facing in terms of:

- Reducing the energy consumption of the data infrastructure by transmitting only relevant data or pre-treated information (countering the unsustainable explosion of the energy demand by data centres and by telecommunication systems requiring higher bandwidths).
- Protecting personal data (GDPR compliance) by local processing and anonymisation of transmitted information.
- Increasing security and resilience due to a reduced reliance on telecommunication links as a result of local decision-making.
- Reducing latency by reducing the quantity of data needed to be transferred to and from a cloud, which is particularly important for automotive, digital society (real-time control of power distribution, for instance) and manufacturing applications, as well as some health applications.

Rethinking human activities to take advantage of the innovation opportunities offered by hyper-connectivity, AI solutions and new kinds of sensors based on miniaturised technologies will create numerous benefits for every new market, ranging from connected cars and digital health to smart home and smart living, and factories of the future. This should include lessons learned from the COVID-19 pandemic like the sudden increase in remote-working.

Sensors and biosensors will be an extensively studied discipline since their rapid, low-cost and highly sensitive features contribute to tremendous advances in many domains. Visible light, IR or multispectral imagers, lidar, radar and ultrasonic sensors, in combination with high-precision inertial sensors, will be essential for the deployment of advanced driver assistance systems (ADAS), augmented reality devices, and industrial automation for instance. Advancements in chemical-sensing technologies also open the

door for multiple new markets. Gas sensors are increasingly integrated into IoT ecosystems to monitor air quality indoors and outdoors – for instance, wearable devices, smart city projects, sensor networks for pollution mapping, smart home electronics and automotive technology. Another key trend to utilise advanced gas-sensing technology is breath analysis, which aims at non-invasive diagnostics via detecting biomarkers from exhaled breath. Furthermore, pressure sensors in human and robot assisted minimally invasive surgery catheters are required to give haptic feedback to the surgeon. Miniaturized ultrasonic sensors open possibilities for minimally invasive medical imaging. However, to access the brain and smaller arteries in the body further miniaturization is required, posing a challenge for current pressure sensor technology.

R&D on highly selective biosensors will contribute to advances in next-generation healthcare, including personalised medicine and the ultrasensitive point-of-care detection of markers for diseases.

Next-generation electronic products are pushing the semiconductor industry to integrate more ultra-thin and flexible ICs. The combination of flexibility and processing capability is very desirable since it reduces weight and enables new form factors, while maintaining desirable functionality such as data logging and RF connectivity. Ultra-thin and flexible ICs enable more efficient and cost-effective solutions that will affect many applications, such as wireless communications, wearable electronics, implantable biomedical devices and the IoT.

The field of quantum sensing is rapidly expanding because quantum phenomena are extremely sensitive to their environment and thus can be used to measure physical properties with unprecedented precision. Quantum sensing refers to the process of employing an individual or an ensemble of quantum systems, often a quantum coherence and/or a quantum entanglement, to measure a physical quantity – ideally with improved accuracy, stability, sensitivity, sensitivity, precision, or spatial resolution compared to conventional measurements.

Quantum sensing usually describes one of the following:

1. Use of a quantum object to measure a physical quantity (classical or quantum). The quantum object is characterized by quantized discrete and resolvable energy levels. Specific examples include electronic, magnetic or vibrational states of superconducting or spin qubits, cold atoms, trapped ions, or photons.
2. Use of quantum coherence (i.e., wavelike spatial or temporal superposition of states) to measure a physical quantity.
3. Use of quantum entanglement to improve the sensitivity or precision of a measurement, beyond what is possible classically.

There are two generations of quantum sensors. The first, which includes devices such as microwave atomic clocks and superconducting quantum interference devices (SQUIDs), has been available for decades. The second generation, which includes atomic clocks, gravity sensors, magnetometers, gravimeters, gyroscopes, nitrogen-vacancy (NV) sensors, and other innovations, is just emerging. Second-generation quantum sensor applications may enable various domains:

- **Biomedical imaging**: neural sensing and heart imaging.
- **Spectroscopy**: imaging of molecular structure such as proteins.

- **Communications**: Signal receiving and amplification for radar communication; calibrating electrical standards to support 5G/6G.
- **Navigation**: Providing high-accuracy GPS; assisting with navigation inside buildings and underground.
- **Environmental monitoring**: Predicting volcanic disruption and measuring CO_2 emissions.
- **Infrastructure monitoring**: Monitoring mechanical stability and detecting leaks.
- **Geographical surveying**: Assisting with the location of oil and gas.

1.1.3 Major Challenges

To achieve application breakthroughs and strategic advantage, the European position must be reinforced through leadership in all relevant equipment, materials, processes and manufacturing technologies by driving the following Major Challenges:

- **Major Challenge 1:** Advanced computing, in-memory, neuromorphic, photonic and quantum computing concepts.
  Materials and substrates, process modules and integration technology for novel devices and circuits for advanced computing, memory and in-memory computing concepts based on nano-electronic, photonic, quantum or other technologies.
- **Major Challenge 2:** Novel sensor, actuation and other devices that enable advanced functionality.
  Materials and substrates, process modules and wafer level integration technology for novel devices and circuits that enable advanced functionality: sensing including quantum sensing, actuating, power conversion, connectivity, etc.
- **Major Challenge 3:** Advanced integration solutions.
  Advanced integration including 2.5/3D integrated devices at wafer level, wafer-to-wafer (W2W) or material on wafer (sequential integration) or dies bonded/attached to a wafer (D2W), etc.
- **Major Challenge 4:** Advanced wafer fab equipment and manufacturing solutions.
  Equipment and manufacturing technologies for processing wafers in fabs from leading edge nodes to differentiated technologies and for advanced functionality devices, including new materials or unconventional geometry and heterogeneous integration technology options.
- **Major Challenge 5:** Advanced packaging, assembly & test equipment solutions.
  Equipment solutions to enable assembly and testing of a wide range of IC's from logic and memory to advanced 2.5/3D integrated devices.
- **Major Challenge 6:** Sustainable semiconductor manufacturing.

1.1.3.1 Major Challenge 1: Advanced computing, in-memory, neuromorphic, photonic and quantum computing concepts

Semiconductor process technology and integration actions will focus on the introduction of new materials and substrates, process modules and integration technology, in close collaboration with the

equipment, materials, modelling/simulation and embedded software communities, to allow for the necessary diversity in computing infrastructure. The applications range from high-performance cloud computing in servers for AI, ML and Gen AI data processing, edge computing/AI, and ultra-low power data processing at the IoT node level up to the highest possible performance. The development of new materials, process modules and their integration in computing systems will be compulsory in order to lower the energy consumption of data transmission and processing (e.g. via new currently investigated computing approaches such as in-memory and neuromorphic computing), or to solve classically unsolvable problems with quantum computing.

1.1.3.1.1 State of the art

The obvious solution for transistors with increased electrical performances is the use of fully depleted devices. The industry has adopted three integration methods: FD-SOI CMOS, FinFET and GAA-style CMOS devices. In chip design it is now embraced that these transistor integration methods enable complementary roles depending on the level of system requirements, ie. cloud-based services, edge computing or extreme-edge device functionality.

FDSOI is a 2D technology based on a thin buried oxide (BOX) layer under the CMOS channel. FDSOI exhibits several advantages, such as reducing the leakage current at standby mode and its higher tolerance against soft errors compared to traditional structures. FDSOI is perfectly suited for ultra-low-power IoT automotive, edge AI and 5/6G SoCs. The leading companies currently produce 18 nm and 22nm FDSOI-based chips. The pilot line on FDSOI will develop 10 and 7nm FDSOI technology nodes to allow a further reduction in energy consumption, while increasing its information processing performances thanks to the integration of embedded non-volatile memories, RF modules and 3D-integration options.

The 3D based FinFET and GAA devices provide high current drive, and hence higher speed, low leakage and, most importantly, less wafer area per transistor than the classic 2D metal–oxide–semiconductor field effect transistor (MOSFET) technology. These new devices are designed and processed to deliver better performance for applications in high- growth markets such as hyper-scale data centres, AI and ML, autonomous vehicles and power-efficient SoCs for the most demanding computer applications. The international industry value chain is pushing production beyond the 2 nm node by moving towards more 3D-stacked FET architectures, and requires solutions in materials and process integration challenges (High-NA EUV, 3D-integration for instance) to realise these novel devices.

Scaling further has recently been demonstrated being possible via the introduction of CFET (complementary FET) or 3D-stacked FET devices. A future sub-2nm advanced System-on-Chip pilot line will enable bringing R&D of this technology to higher maturity, including design enablement that will offer access to the European manufacturing and design Industry. This allows SME’s and start-ups to be competitive and strengthen EU’s position in the value chain, increasing the resilience and maintain relevance in the world race of addressing the ever-increasing user needs and societal challenges.

A clear differentiation between logic, memory and process information in conventional von Neumann computing schemes necessitates the frequent movement of data between the memory and processor.

Thus, much of the execution time and energy consumption is spent in the movement of data, a barrier referred to as the “von Neumann bottleneck”, or “memory wall”. This obstacle has been greatly exacerbated since the advent of data-intensive computing applications, such as ML and Gen-AI. Near-memory and in-memory computing are new paradigms, wherein the computing system is redesigned to process data at its storage – in the memory – thereby minimising the expensive movement of data.

Near-memory computing involves adding or integrating logic (e.g. accelerators, very small cores, reconfigurable logic) close to or inside the memory. Logic cores are usually placed inside the logic layer of 3D-stacked memories or at the memory controller.

Silicon and organic interposers allow separate logic chips to be placed in the same die package as a 3D-stacked memory while still taking advantage of the through-silicon via (TSV) bandwidth. Some foundries (Intel, Samsung, TSMC, etc.) offer this kind of heterogeneous integration.

Recent advances in heterogeneous integration technology focus on integrating Si-bridges to connect dies together over very short distances along the die perimeter (e.g. Intel EMIB technology, TSMC implementation of SoIC and “CoWOS” technology).

These heterogeneous integration technologies (Interposers, bridges, chiplets) are often referred to as 2.5D as they still place active die next to each other in a 2D plane. Through 3D integration technology stack active devices are placed vertically on top of each other. This is commonly done in the field of CMOS image sensors and HBM (High Bandwidth Memory) DRAM stacks. These 3D integration technologies use TSV technology in the active die, in combination with high-density die-to-wafer or wafer-to-wafer interconnect technologies. This greatly increases the number of functional interconnects per die area on the functional chips. 3D-Interconnect pitches below 5 µm and even down to 400 nm have already been demonstrated.

An even denser 3D interconnect technology could be achieved by so-called “monolithic” 3D integration, a technique using sequential manufacturing of multiple layers of active devices and high density (Back-end of line) interconnect layers. Such monolithic integration is not currently available in foundries.

The amount of data processed in the cloud, the development of Internet-of-Things (IoT) applications, and growing data privacy concerns force the transition from cloud-based to edge-based processing. Limited energy and computational resources on edge push the transition from traditional von Neumann architectures to In-memory Computing (IMC), especially for machine learning and neural network applications. IMC also uses the intrinsic properties and operational principles of the memory cells and cell arrays, by inducing interactions between cells such that they can perform computations themselves. IMC aims to improve the energy efficiency of artificial/deep neural networks (ANN/DNN) hardware realizations by computing weighted-sum tasks in the memory arrays, for instance.

In an ANN chip, the neuron/synapse states are encoded as digital bits, clock cycles or voltage levels, while in a spiking neural network (SNN) chip, information is encoded into spike timing, to really mimic the biological brain operations. SNN hardware realizations are engineered to seek ultra-low power consumption and run at relatively low frequencies to emulate realistic biological behaviours, referred to as neuromorphic computing.

Due to the increasing need for large memory systems by modern applications (big data analytics, AI, etc.), dynamic random-access memory (DRAM) and Flash memory scaling is being pushed to its practical

limits. It is becoming more difficult to increase the density, reduce the latency and decrease the energy consumption of conventional DRAM and Flash memory architectures. 2D-NAND became monolithically integrated 3D-NAND, found the 3rd dimension for scaling, and DRAM currently follows the same path. This will seek innovation in DRAM select transistor channel material (ALD MX_2, ALD Oxide Semiconductor etc.), capacitor dielectric, new cell architecture, new process steps etc. Alternative approaches are also being developed to overcome these barriers for implementing near- or in-memory and neuromorphic computing.

The first key approach consists of stacking multiple layers of memories (DRAM, Flash). With current manufacturing process technologies, thousands of TSVs can be placed within a single 3D-stacked memory chip. The TSV provide much greater internal memory bandwidth than the narrow memory channel. 3D-stacked DRAM and Flash are also commercially available.

The second major innovation is the use of emerging non-volatile memory (NVM) as parts of the main memory subsystem, and as embedded memories. New memory devices and technologies that are currently being investigated can both store data at high densities, lower costs, and present other benefits that will help computation with new in-memory computing paradigms: fast access time, long data retention, multilevel to analog ability and/or high endurance. The main emerging NVM technologies to allow in-memory computing architectures and embedded memories are: (i) phase-change memory (PCM), Threshold Change memory (TCM) ; (ii) magnetic RAM or spin-transfer or spin-orbit torque, or voltage-controlled magnetic anisotropy magnetic RAM (MRAM, STT-MRAM, SOT-MRAM, VCMA- MRAM); (iii) metal-oxide resistive RAM (RRAM or ReRAM) and conductive-bridge RAM (CBRAM) or memristors; (iv) ferroelectric FET (FeFET), RAM (FeRAM) and tunnel junctions (FTJ); (v) Electrochemical RAM (ECRAM) and (vi) Oxide Semiconductor (OSC) channel gain cell (2TnC, n=0 or 1). All these NVM types are expected to provide memory access latencies and energy usage that are competitive with- or close enough to- DRAM, while potentially enabling much larger non-volatility in main memory, and enabling new functionalities for computing systems outside Von Neuman architectures.

Thanks to its optimal compatibility to CMOS technology, Silicon Photonics is becoming a key material platform enabling technology for high-speed connectivity in data centres. In the near future, Photonic Integrated Circuits (PIC) can also bring significant changes to high-performance computers and unlocking the full potential of AI by resolving the transmission limits of electronics.

Photonic processors, that compute with photons instead of electrons, display some extraordinary properties, such as an ultra-wide communication bandwidth, ultra-high processing frequency, and ultra-low energy consumption. Additional dimensions division multiplexing of light field such as wavelength and spatial mode enable multithread processing with almost no extra computing overhead, leading to a significant acceleration against traditional electronic computers.

By combining the high bandwidth and parallelism of photonic devices, photonic neural networks (PNNs) have the potential to be orders of magnitude faster than state-of-the-art electronic processors while consuming less energy per computation. PNNs aim to leverage high-speed optical devices to mimic essential computing primitives (neurons and synapses) and connect them into a neural network (ANN/SNN) with highly parallel and dense optical interconnects.

The goal of neuromorphic photonic processors is not to replace conventional computers, but to enable applications that are unreachable at present by conventional computing technology in terms of low latency, high bandwidth and low energies.

Photonic processors have light sources, passive and active devices. Nowadays, more than 10 companies produce PICs worldwide, mainly based on SOI wafers. However, there is no commercial fabrication platform that can simultaneously offer devices for light generation, optical amplification, wavelength multiplexing, photo-detection, and transistors on a single die. State-of-the-art devices in each of these categories use different photonic materials (SiN, Ge, InP, GaAs, 2D materials, etc) with incongruous fabrication processes (SOI, CMOS, FinFETs).

Energy efficient and fast switching optical and electro-optical materials are needed for non-volatile photonic storage and weighing (synapses), as well as high-speed optical switching and routing, with low power consumption. Neural non-linearities are already possible on mainstream platforms using electro-optic transfer functions, but new materials promise significant performance opportunities. Phase change materials (PCMs), graphene and ITO-based modulators can also be utilized for implementing non-linearities (neurons).

On-chip optical gain and power will require co-integration with active III-V (InP or GaAs) lasers and semiconductor optical amplifiers. Current approaches involve either III-V to silicon wafer bonding (heterogeneous integration) or co-packaging with precise assembly (see also Chapter 1.2). Quantum dot lasers are another promising approach as they can be grown directly onto silicon, but fabrication reliability does not reach commercial standards today. Co-integrating CMOS controller chips with silicon photonics to provide electrical tuning control/stabilization, and robust packaging to prevent PIC temperature fluctuations, will be critical.

The past decade has seen an explosion in efforts to develop quantum computers that could revolutionize the fields of physics, medicine, biology, AI, finance and cryptography by exponentially speeding up certain computational domains. While such demonstrations certainly mark an essential technological milestone, tasks accomplished at such an unimaginable speed do not necessarily prelude the commercialization of quantum computers in the short term. To ensure the continued progression of quantum technologies over the next decade, advances in materials and fabrication processes are required for quantum computing hardware, following a path similar to the transistor technology scaling that enabled the evolution of digital computing.

1.1.3.1.2 Vision and expected outcome

Driven by market demand, on the one hand for advanced high-performance computing, AI/ML, and on the other hand for mobility, edge AI and IoT devices, the advanced Si technology roadmaps for both FinFET/GAA and FDSOI will need to be pushed further. To enable this, a wealth of explorations into novel low-thermal-budget-processing 2D materials, nanowires, nanosheets or nanoribbons and quantum dots needs to be combined with significant developments in advanced 3D integration schemes of materials and devices. In parallel, to overcome the von Neumann bottleneck, development of new computing paradigms such as neuromorphic, in-memory, photonic and quantum computing is essential.

New memory concepts will support the correct memory hierarchy in various applications. An example here is the opportunity to push new memory concepts (resistive RAM (RRAM), phase-change RAM (PCRAM), Thresholds Change RAM, STT-MRAM, FeFET, FeRAM, FTJ, Electro-Chemical RAM (EC-RAM)) to the demonstration level in the IoT infrastructure (from server, over edge to nodes). These alternative memories require the development of advanced novel materials (magnetic, phase-change, nanofilament, ferroelectric, electrochemical). A much closer collaboration between new material innovation, process, device integration, device teams and system architects, is indispensable in the future. New markets will require storage class memory to bridge the performance gap between DRAM and NAND Flash. Edge AI and IoT applications will require low-power embedded devices and cloud computing with more mass-storage space. The standard memory hierarchy is challenged. Indeed, learning algorithm requirement will dramatically increase the requirements on memories densities, access bandwidth and endurance on one hand, while new functionality - such as Multilevel to analog non-volatile memory cells - are required to allow efficient in memory computing approaches like ANN, from direct matrix vector multiplication to CNN or spike neural architectures. Simultaneously, advanced interconnect, System on Chip (SoC) integration issues will need to be addressed (cf. also Major Challenges 2 and 3), with innovative solutions to reduce costs being required. The option to use advanced 3D and optical input/output (I/O) technological solutions, to circumvent limitations of traditional I/O architectures, are strengths to foster and build upon in Europe.

Furthermore, the downscaling of photonic components (light sources, modulators, photodetectors, optical phase shifters…) and their integration on CMOS platforms would lead to photonic neural networks (PNNs) for overcoming the current memory bottleneck. Such PNNs are expected to achieve orders of magnitude enhancement in energy efficiency and throughput compared to ANNs and SNNs. Hence, the intimate collaboration between the strong EU electronic and photonic communities would enhance the EU leadership in this domain.

One of the current major issues for most of the developed quantum technologies is their future scalability. For example, quantum computing error rates multiply as scale increases, and creating large numbers of qubits that are stable enough for long enough is extremely challenging. Collaboration between quantum “laboratories” and the EU electronic industry looks compulsory for strengthening the EU force in quantum computing.

To maintain the European competencies in advanced design for integrated circuits and systems, a close link with a strong effort in semiconductor process technology and integration has to be maintained. Issues such as the creation of standards for the IoT, reliability for safety or mission-critical applications, security and privacy requirements need close collaboration among all players to build leadership going forward in this coming generation of advanced and distributed computing infrastructure and diversified system performance.

Expected achievements

Maintaining competence on advanced logic and memory technology in Europe is key to maintaining strategic autonomy and supporting societal benefits from the core technology base. Implementation of dedicated and sustainable pilot lines for specialised logic processes and devices supporting European critical applications is also a major objective, as is the exploration of new devices and architectures for low-power or harsh environment applications.

1.1.3.1.3 Key focus areas

This challenge includes the following key focus areas:

Topic 1.1

- Explorations of the scaled Si technology roadmaps of the 2 and 1 nm nodes including FinFET/Trigate and stacked gate-all-around horizontal or vertical nanowires, Forksheet-, complementary FET architectures, next generations FDSOI, 3D integration, and further device and pitch scaling, where parallel conduction paths (nanowires, nanosheets, nanoribbons, etc.) are brought even closer together. It includes novel device-interconnect technology such as - but not limited to - contact from wafer backside.

Topic 1.2

- Exploration and implementation of materials beyond Si (SiGe, SiC, GaN, Ge, InGaAs, InP, functional oxides, 2D material heterostructures, CNT and nanowires).
- Unconventional devices and materials, such as 2D and III-V materials, oxide-semiconductors, metamaterials, metasurfaces, nanowires, CNTs, nanosheets, nanoribbons, nanoparticles, quantum dots, spin effects, functional oxides, ferroelectric and magnetic, which are being investigated to overcome the limits of conventional CMOS logic and memories.

Topic 1.3

- Novel device, circuit and systems concepts for optimum PPAC specifications, high-energy efficiency and novel paradigms such as for near/in-memory, neuromorphic, optical and quantum computing.
- New Photonic integrated circuits (PIC) for a further improvement of optical I/Os for enabling compute, memory, and networking ASICs to communicate with dramatically increased bandwidth, lower latency and at a fraction of the power of existing electrical I/O solutions.
- In a longer term, Photonic Neural Networks (PNNs) could bring the benefits of photonics over electronics (energy efficiency, low latency, higher bandwidth, parallelism…) to AI/ML.

Topic 1.4

- Long-term challenges such as steep slope switches (tunnel FET, negative capacitance FET, nanoelectromechanical systems / NEMS), spin-based transistors, and alternative high-performance switches.

Topic 1.5

- New embedded non-volatile memory (eNVM) technologies to enable local AI processing and storage of configuration data, which decrease data transmission volume, energy needs and allows for more efficient control of electric powertrains and batteries, along with many other applications in the IoT and secure devices domains.

1.1.3.2 Major Challenge 2: Novel sensor, actuation and other devices that enable advanced functionality

Materials and substrates, process modules and wafer level integration technology for novel devices and circuits that enable advanced functionality: sensing - including quantum sensing -, actuating, power conversion, connectivity, etc.

1.1.3.2.1 State of the art

Besides the highly integrated chips necessary to overcome Major Challenge 1 on advanced computing, memory and in-memory computing concepts, many more devices are needed to achieve advanced functionalities – such as sensing and actuating, power management, and interfaces to other systems. This is what has also been named “More than Moore”, and is an integral part of all systems, as well as one of the strengths of European microelectronics. Given the inherently diverse nature of this sector, the state of the art will be captured by providing a few snapshots of key technologies.

For IoT applications, logic and RF functions are combined, but not with the highest efficiency required by the ultra-long lifetime of unattended objects. Energy harvesting schemes, often based on photovoltaics, do exist, yet are not always able to provide the requested energy supplement of self-contained low-volume and low-cost sensor nodes.

Smart optical, mechanical and magnetic sensors are already able to provide a wealth of information for complex systems. Nevertheless, there are current limits to integrating various types of sensors monolithically. In the field of optical sensors, for instance, depth mapping requires complex scanning schemes using either mechanical systems or large volume and poorly integrated light sources. Devices based on rare or expensive materials, which are not compatible with standard CMOS technology, cover various useful zones of the electromagnetic spectrum. The same is true for chemical-sensing technologies, which are mostly based on metal oxides or other coated materials. While solutions for specific gases and applications are starting to emerge, sensitive and robust technologies using semiconductors still remain to be developed for a large number of applications and species, or to enhance the performance in concentration ranges, selectivity and stability. The situation is similar for many kinds of sensors and actuators. For instance, fine pitch displays are beginning to be possible, but will require new advances, both in high brightness / low variation sources and assembly methods.

Technologies used for the next generation of quantum sensing include neutral atoms, trapped ions, spin qubits, superconducting devices, and photonics. Please note that in the previous sentence “quantum sensing” means: sensing using individual quantum objects and their entanglement. They can be used to measure the magnetic field (B), the electric field (E), the rotation (θ), the acceleration (g), the time (t), the frequency (f), the temperature (T), the pressure (P), the force (F), the mass (m) and the voltage (V) (Table 1). Charged systems, like trapped ions, will be sensitive to electrical fields, while spin-based systems will mainly respond to magnetic fields. Some quantum sensors may respond to several physical parameters.

In the more conventional light sensing techniques, sensors are often based on the absorption of a given semiconductor species, which leads to a rather broad but limited energy range. Emerging techniques to

tailor the wavelength range by either confinement of the sensing element (“quantum dots”) or the combination of different materials in the same stack. The question of wavelength selection, in case a further wavelength selectivity is needed - for instance to address both the visible and near infrared bands - is usually addressed by stacking different sensing elements and optical filters of various principles.

In power technologies, recent years have seen the emergence of wide bandgap materials able to reduce the losses of power conversion, namely SiC and GaN, or other wide bandgap technologies. These technologies are making quick inroads as one of the cornerstones for the energy transition, and are becoming dominant in some sectors, like high-power electric motors... However, they are still nascent, and the challenge is to develop low-cost (involving larger diameter, good quality and less-expensive substrates) and robust technologies. Today, SiC is produced mainly on 150 mm substrates, while some GaN devices are produced on silicon substrates, but the technology and epitaxy techniques will still need further refinement (and even breakthroughs). Moreover, the development of disruptive substrate technologies as well as layer transfer will be key steps toward a cost-effective, high-performance solution linked with transition to 200 mm, then from 200 mm to 300 mm substrates where possible and where volumes justify it. This is essential for future integrated logic and power management functions using technologies combining logic and power transistors. Besides research on wide bandgap materials, the Si-based insulated-gate bipolar transistor (IGBT) technologies have further innovation potential in the area of cost-sensitive applications. Challenges are in the domain of high-power and high-voltage electronics with high junction temperatures processed towards larger diameter substrates – leading to increased power densities and lower costs to support the transformation in the energy systems with Si-based power semiconductors. In some cases, the power dissipation of the devices - which remain high despite their better efficiency - is a real challenge and needs to be addressed both at device and wafer level and at the packaging level (see also Chapter 1.2).

For RF and communication technologies, recent advances in integrating RF technologies on low-loss substrates such as SOI have allowed the integration of switches as well as amplifiers on the same silicon substrates. This concept is in production in Europe on 200 mm and 300 mm wafer substrates. Further advances are on the way on both substrate diameters, which will allow the integration of more functions and address the requirements of complex 5G systems below and beyond 6 GHz, up to the mm waveband. Synthetic antennae systems for radar or communications are emerging thanks to highly integrated RF technologies, including BiCMOS, but are often limited by power consumption and costs. For example, BiCMOS brings advantages over some III-V technologies for some applications, leveraging the capability to integrate digital functions. For sure, it cannot compete with GaN when very high power is requested, but GaN can neither compete with BiCMOS for the products requiring mixed-signal functions. New, RF technologies delivering high output power and efficiency like RF GaN (GaN-SiC as well as GaN-Si) and other III-V based materials - such as InP - could overcome these limitations. Those technologies have to be considered either stand-alone or in combination with either RFCMOS or BiCMOS using heterogenous integration. In the field of communications, the integration of photonics technologies with electronics is gaining commercial ground. Further advances in efficient source integration, and modulation and power efficiency, are still needed to use them more widely. New advances in fine photon handling can also open the way to innovative sensing techniques, either by using light interaction with the signal to be measured outside the PIC and sensing the effect of this

interaction within the PIC, or by using the PIC as an actuator, for instance implementing optical (phased array) antennae.

In optical communications, the intrinsic capability of light waves to transmit signals with low latency and power dissipation, at ultra-high data rates, can be scaled from long-haul infrastructures to intra-datacenter optical links, down to chip-to-chip photonic interconnects. However, bulk silicon cannot meet the necessary requirements of these integrated optics applications which can be addressed with silicon-on-insulator (SOI) technology. SOI photonics, which is part of Silicon Photonics, is one route to enable the development of novel lidar systems as well as support advancements in quantum technologies. By leveraging mature semiconductor manufacturing methods, engineered wafers that incorporate SOI technology offer a powerful approach toward broader adoption of advanced chip-scale integrated optics. In addition to substrate progress a host of innovations will be necessary - and are expected - to boost the (Silicon) Photonics Integrated Circuits (PIC). Among those are new generations of active devices including the heterogeneous integration of active devices (sources, modulators) or passive components and detectors (mainly for sensing), for example for wavelengths outside the communication frequencies. They involve new materials and integration techniques.

In “traditional” polyimide (PI)-based flexible electronics, the continuing trend is towards more complex designs and large-area processing, especially in displays and sensor arrays. Since the achievement of high-performing flexible electronics by monolithic approaches is limited, hybrid approaches are used when conventional electronics (such as thinned chips) is assembled on flexible electronic substrates. For more complex devices, the reliability and performance of organic materials or mechanical and processing properties of inorganic materials are still a focus of research activities in addition to adapted and optimised assembly techniques. In general, current R&D activities indicate that technical spots can be identified where a merging of novel flexible devices and adapted Si electronics create progress beyond the state of the art.

1.1.3.2.2 Vision and expected outcome

Depending on the application, the advantages of More-than-Moore (or SoC) technology are size, performance, cost, reliability, security and simpler logistics. Therefore, this approach is a key enabler for the European industry. To maintain and strengthen Europe’s position, it is necessary to improve existing technologies, and to seamlessly integrate emerging technologies in a reliable and competitive way. All application domains addressed by the ECS SRIA will benefit from components with very diverse functionalities.

Specific process technology platforms may be required, as in the case of biomedical devices for minimally invasive healthcare or point-of-care diagnosis, or mission-critical devices in automotive, avionics and space. Semiconductor process and integration technologies for enabling heterogeneous SoC functionality will focus on the introduction of advanced functional (nano-)materials providing additional functionalities and advanced device concepts.

Innovations for these domains require the exploration and functional integration, preferably in CMOS-compatible processing, of novel materials. A non-exhaustive materials list includes wide bandgap materials, III-V semiconductor compounds, 2D materials (e.g. graphene, MoS_2 and other transition metal dichalcogenides), 1D (e.g. nanowires, carbon nanotubes) and 0D (e.g. nanoparticles, quantum dots)

materials, metal oxides, organic semiconductors, ferro- and piezoelectric, thermoelectric and magnetic thin films materials, materials with specific properties (for optics: dielectrics, bi-refringent, phase change materials which can also be used for conductivity change properties, for electromagnetic properties: low permittivity, etc..), metamaterials and metasurfaces. Obviously, safety and environmental aspects should also be taken into consideration.

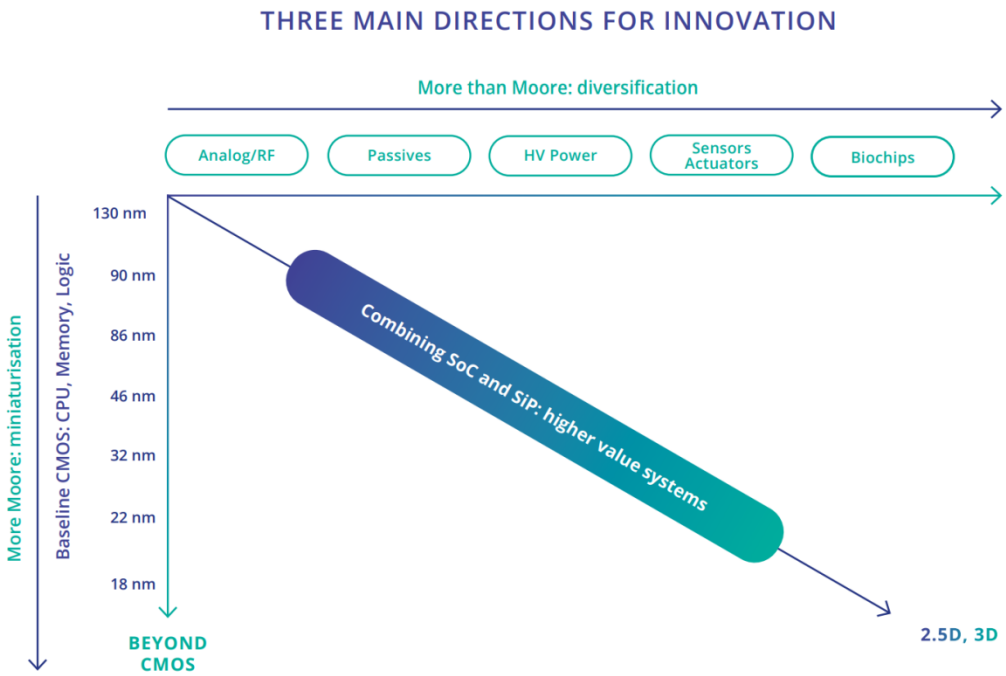

Figure 1.1.3 Diversification of applications, continued miniaturisation and integration on chips and in package leads to higher value systems (Source: ST Microelectronics/IRDS)

The driver for SoC integration is always a clear demand from the application domain. To maintain and push forward Europe's position, the focus should be on emerging technologies as they are introduced, as well as new developments in the equipment and materials industry, in which Europe has a leading position. Furthermore, the early generation of models and their initial validation for benchmarking and intellectual property (IP) generation are required to reinforce position of Europe in specific design concepts and architecture, especially when used in combination with re-use IP and third-party IP blocks to secure fast time to market.

Expected achievements

This will involve the implementation of pilot lines for integrated application-defined sensors, novel IoT solutions, complex sensor systems and new (bio)medical devices, new RF and mm-wave device options (including radar and sensing), much more efficient power management, higher integration of passive devices, photonics circuits and options, novel and more efficient displays and electronics, this list being non exhaustive. Key will be the initiation of process technology platforms for the exploration and exploitation of advanced functionalities through integration of novel reliable materials.

The exploration and implementation of materials beyond Si will require strategic collaborative EU projects for European industry to become more independent, and will result in the development of an EU-based supply chain for wide-bandgap materials, for example, including a move towards larger substrate sizes of 200 and 300 mm (i.e. SiC and GaN, and also InP which provides a further challenge to GaN in that it cannot be grown on Si).

1.1.3.2.3 Key focus areas

More specifically, the following challenges are identified (this is a non-exhaustive list).

Topic 2.1: Application-specific logic: as explicitly treated in sub-section 1.1.4.3, heterogeneous SoC integration can require specific solutions for logic to be integrated with More-than-Moore technologies such as the following:

- Logic integration with RF, optical or sensor technologies.
- Integration of lasers and detectors within silicon photonics platform.

Topic 2.2: Advanced sensor and actuators technologies:

- Mechanical sensors (e.g. acceleration, gyroscopes, microphones).
- Chemical sensor devices such as selective gas-sensing components for environmental monitoring or smart medicine and smart health (e.g. CO, CO_2, NO_x, O_3, toluene, VOCs, acetone, H_2S, etc…).
- Physical sensors (magnetic, optical, RF).
- Multispectral or highly sensitive optical sensors.
- Transmitter/receiver technologies for applications such as lidar and active phased array imaging.
- Biomedical and biochemical sensors.
- New - more efficient - displays, in particular micro displays.

Topic 2.3: Advanced power electronics technologies (Si-based, BCD, SiC, GaN, Ga_2O_3, AlN etc.) to enhance the efficiency of motors, energy storage, lighting systems, etc. More specifically:

- Higher power density and frequency, wide-bandgap materials for high temperature electronics, new CMOS/IGBT processes, integrated logic, uni- and bipolar; high voltage classes, lateral to vertical architectures.
- Materials for energy harvesting (e.g. perovskite solar cells, piezoelectric ceramics and thin films) and storage (e.g. perovskites, ferroelectrics and relaxors), micro-batteries, supercapacitors and wireless power transfer.
- Power devices and modules for highly demanding automotive, industrial and energy infrastructure applications.
- Substrates towards larger diameters to serve future greater demand for cost-sensitive power solutions.

Topic 2.4: Quantum sensor technologies:

- Atomic vapor or cold atom (Bose-Einstein condensate) based sensors.
- Trapped ion-based quantum sensors.

- Solid state spin-based quantum sensors making use of Nitrogen-Vacancies or color centres as sensitive element.
- Superconducting circuit sensors based on SQUIDS, flux qubits and charge qubits.
- Sensors based on photon entanglement using nonlinear optical media.

Topic 2.5: Advanced RF and photonics communication technologies to interface between semiconductors components, subsystems and systems. These technologies should enable better and more energy-efficient control of emission and reception channels (for example, for 5G connectivity and 6G) via:

- New energy-efficient RF and mm-wave integrated device options, including radar (building on e.g. SiGe/BiCMOS, FD SOI, CMOS, GaN or other III-V compounds, PIC).
- Development and characterisation of new RF cryogenic electronics for Quantum Information Processing (QIP), as well as logic devices at quantum-enabling cryogenic temperatures, taking into account the available cooling power of refrigerators and interfacing requirements at different operation temperatures.
- Energy-efficient computing and communication, including a focus on developing new technologies.
- Bringing MOEMS and micro-optics, nanophotonics, optical interconnections, photonics-enabled device and system options into a CMOS-compatible manufacturing flow.

1.1.3.3 Major Challenge 3: Advanced integration solutions

Advanced integration including 2.5/3D integrated devices at wafer level, wafer-to-wafer (W2W) or material on wafer (sequential integration) or dies bonded/attached to a wafer (D2W), etc.

By splitting the chip into smaller functional physically separate parts, the overall system yield improves and system performance is enhanced. In addition, by using system-independent IP block design and verification, as well as common die-to-die interfaces (including IP re-use and use of third-party IP), a faster time to market can be achieved. One counterpart being that the design and testing strategy needs to be entirely revised in order not to lose the yield advantage, and that assembly costs (as collective as possible) and yields must also be mastered. This is the key overarching challenge of this approach.

1.1.3.3.1 State of the art

Over the last few years, a huge variety of semiconductor products have emerged where several functions are added in one IC, enabled by advances in integration technology. This is the so-called System in Package (SiP) approach.

To maximise the benefits from ICs made of small geometry nodes, below 40 nm typically, and certainly as of 7 nm and less, there has already been a move to more advanced methods, to manage complexity in the most cost-effective way. These advanced integration methods involve technologies such as flip chip, but also - depending on the use cases - wafer-level packaging, fan-out wafer-level packages without substrate interposers and complex 3D structures with TSVs, micro-bumps and thin dice.

The functional diversification of technologies, where digital electronics meets areas such as analog, photonic and MEMS technologies, has been advanced through the assembly of heterogeneous elements. For example, in today's power stages in automotive powertrain applications, power modules integrate several dice in parallel. Similarly, 5G networks are enabled by advanced RF functionality, often combining a photonic interface with in-package integrated logic and memory functionalities. Semiconductor materials encapsuled in packaging technology have already moved from being largely silicon-based or based on III-V compounds for photonic or high-power RF applications, to more advanced SiC and GaN compounds. On the part of the package, the industry has moved towards environmentally friendly lead (Pb) and halogen-free moulding compounds. For wire bonding, a similar move from aluminium and gold towards copper and silver wiring has been made. Furthermore, flip chip attach has made a transition to lead-free bumps (inside the package) and BGA using lead-free balls (at the interface between the package and the board) materials.

1.1.3.3.2 Vision and expected outcome

This challenge covers the integration of new chip technologies in advanced low parasitic packages, as well as chips of different functionalities resulting from the previous two challenges – e.g. CMOS logic, NVM, NEMS/ MEMS, RF, analogue, sensing, actuating, optical, power management, energy harvesting and storage – into a SiP.

Depending on the application and type of system, the key drivers and parameters to be improved can be the density of contacts, the parasitics, the integration of passives - including antennae -, the thermal dissipation, the optical quality, the number of dice to be integrated either horizontally or vertically, the ability to handle various environmental conditions, including extreme temperatures or resistance to chemicals, etc. ..It is becoming more and more clear to everyone that the overall performance of the system is dependent not only on the semiconductor technologies but also - and sometimes in equal part, or even predominantly - on the integration technology.

Advanced integration technologies are required for mm-wave applications (> 30 GHz), both GaN/Si RF and other high-electron-mobility-transistor (HEMT) devices, or dedicated MEMS and sensor devices (e.g. electro-optics for lidar without moving parts). Depending on the application, heterogeneous integration technology can provide a better compromise between available functions, performance, cost and time to market.

System integration technologies are a key enabler for the European industry, including for instance the essential field of energy transition with power management devices, but also longer term evolutions, like the new field of cryogenic QIP, characterisation of logic devices at quantum-enabling cryogenic temperatures, and associated packaging challenges. To maintain and strengthen Europe's position, it is necessary to improve existing technologies and develop emerging technologies, as well as to integrate both to advanced electronic systems in a competitive and reliable way. All application domains addressed by the ECS agenda will benefit from innovative integration technologies.

Moreover, component carriers also known as Integrated Circuit (IC) Substrates represent a big portion of the package cost (up to 50%), excluding the semiconductor component itself. This is particularly true for Flip Chip Ball Grid Array (FC-BGA) Substrates, which are essential component carriers in high-performance, high-interconnect density computing solutions. Due to the increase of functionality and driven by chiplets

integration, FC-BGA substrates are facing many challenges, not only in terms of miniaturization, but they are also becoming central elements for thermal management in advanced computing systems.

Integration of the above functionalities in miniaturised packages and (sub)SiP require fundamental insights into application needs and system architecture. Process and characterisation technology to realise this integration is part of this third Major Challenge, and is essential for ensuring Europe's prominent role in supplying novel solutions for the various existing and emerging application domains.

At the macro-scale level, a system consists of a collection of large functional blocks. These blocks have quite different performance requirements (analogue, high voltage, eNVM, advanced CMOS, fast static RAM (SRAM), multi-sensing capability, etc) and technology roadmaps. Therefore, for many applications it is of increasing interest to split the system into heterogeneous parts, each realised by optimum technologies at lower cost per function, and assembled with parts using high-density 3D interconnect processes. In other words, for each application or system the SoC / SiP trade-offs and partitioning have to be revisited in the light of the respective evolutions of base technologies.

It is clear that 3D integration in electronic systems can be realised at different levels of the interconnect hierarchy, each having a different vertical interconnect density. Different technologies are therefore required at different levels of this 3D hierarchy.

For the reasons above the Electronic Design Automation of 3D integration is to be much further explored and constitutes a very challenging domain as described in Chapter 2.3.

1.1.3.3.3 Key focus areas

Research and development priorities are focused on innovative approaches, such as the following.

Topic 3.1: Advanced Si interconnect technologies:

- Interconnect technologies that allow vertical as well as horizontal integration: this includes process technologies for vertical interconnects, such as TSV, through-encapsulant via (TEV), through-glass via technologies and microbumps, and copper/copper bonding, as well as process technologies for horizontal interconnects such as thin film technologies for redistribution on chips.
- Implementation of advanced nanomaterials and metamaterials, including low-thermal-budget-processing 2D materials, nanowires, nanoparticles and quantum dots with scalable logic and memory device technologies.
- New materials to maximize efficiency of the Package Thermal dissipation (Flip Chip Thermal Enhanced BGA) is required to deal with the very demanding computing applications in extreme conditions i.e. Automotive, space environment.
- New materials like Al bumps from Electroplating could solve reliability issues and ensure advanced CMOS compatible integration.
- Power electronic substrates will benefit from thick Al layers fabricated by novel electroplating technologies and other thermal redistribution techniques.

Topic 3.2: Specific sensing and actuation technologies.

- Solutions for advanced optical functionalities on wafer, either for sensors (visible, NIR, infrared), or for PIC.
- Specific solutions for the signal conditioning of other sensors (mechanical, physical, chemical…).
- Increasing functionality in IC Substrates for high efficiency power delivery including voltage regulator circuitry and integrated capacitances and other passives.

Topic 3.3: 3D integration technologies:

- High-integration density and performance-driven 3D integration (power/speed). For this category, denser 3D integration technologies are required: from the chip I/O-pad level 3D-SIP, to finer grain partitioning of the 3D-SOC and the ultimate transistor-level 3D-IC (see Sub-section 2.3.1 for the 3D landscape).
- Chip-package-board co-design. This will be of utmost importance for introducing innovative products efficiently with a short time to market (and which is closely linked to the work described in Section 2.2).
- System integration partitioning: the choice of 3D interconnect level(s) has a significant impact on system design and the required 3D technology, resulting in a strong interaction need between system design and technology with a significant impact on electronic design automation (EDA) tools.

System requirements and semiconductor device technology (Major Challenges 1 and 2) will evolve at the same time, creating momentum for further interconnect pitch scaling for 3D integration technology platforms. Hence, the timelines of all four challenges of this section are strongly connected.

1.1.3.4 Major Challenge 4: Advanced wafer fab equipment solutions

This is about equipment and manufacturing technologies for processing wafers in fabs, from leading edge nodes to differentiated or mature technologies and for advanced functionality devices, including new materials or unconventional geometry and heterogeneous integration technology options.

The semiconductor equipment and manufacturing sector in Europe provides the global market with best-in-class equipment to enable the manufacturing of miniaturised electronic components. The European equipment industry, RTOs and small and medium-sized enterprises (SMEs) active in this sector have a long history of successful mechanical engineering, tailor-made machinery, optical equipment, metrology, inspection and testing equipment, and chemical processing tools. This history of success is prominent in several domains, foremost in lithography (in particular EUV) and metrology, but also in thermal processing, deposition, etching, cleaning and wafer handling.

1.1.3.4.1 State of the art

At the forefront of semiconductor manufacturing equipment is the production of logic and high-performance memory, which are applied mainly in portable devices as well as advanced cloud computing and data storage facilities. The continuous increase of device density known as Moore’s law

is being driven by an ability to create ever-smaller features on wafers. The technology leaps required to keep up with Moore's law have already been achieved via additional roadmaps complementing ongoing 2D pattern size reductions. They are realised by combining various devices, materials, and 3D and system architecture aspects that required dedicated long-term investment in high-tech equipment solutions. Enabled by current deposition, lithography, etch, processing and metrology tools and their performance, the 3nm technology node is in production by market leaders, solutions for 2nm node are planned for 2025[4], and even Angstrom nodes[5] are being explored.

For the production of miniaturised and reliable More-than-Moore electronic components and systems, such as sensors and sensor systems, MEMS, advanced imagers, power electronics devices, automotive electronics, embedded memory devices, mm-wave technologies, and advanced low-power RF technology, many equipment and manufacturing solutions have been implemented.

1.1.3.4.2 Vision and expected outcome

The ever-increasing demand for leading-edge logic and memory technology is driving the development of new equipment and material solutions for sub-2 nm node semiconductor technologies. Besides finding equipment solutions for further shrinking minimum feature sizes well below 1 nm, the alignment accuracy of successive layers, called "overlay" or in another definition type "Edge Placement Error", needs to move towards Angstrom levels in a process technology roadmap that combines complex materials in 3D structures and architectures. At the same time, productivity demands on the equipment continue to increase to maintain reduced overall production costs. Process yield also continues to be a challenge with shrinking feature size and the increasing impact of defects and contamination.

In the realm of cutting-edge technology, the advent into new nodes necessitates the development of novel materials. These materials are either integrated into the structure to enhance electrical properties or utilized as sacrificial elements to facilitate the creation of intricate 3D shapes. The precision in material deposition is becoming increasingly critical, requiring meticulous control over where materials are applied, their thickness, and whether they are deposited on horizontal or vertical surfaces.

The semiconductor industry is driven by the dual goals of boosting productivity and slashing energy and water consumption. Wafer fabs are striving to process more wafers per hour without increasing power usage, achieved through enhanced equipment throughput, real-time optimization of production flows and streamlined processes. Despite variations in throughput across different equipment types—such as lithography's DUV throughput at approximately 295 wafers per hour, whereas throughput in deposition might take up to a few minutes for single wafer processes—there is a universal push for higher throughput and yield, alongside refined process control to minimize additional steps and reduce defective wafers. This pursuit has led to the development of more sophisticated equipment in patterning, processing and metrology, with kWh/wafer serving as a pivotal metric for sustainable innovation.

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[4] TSMC 2nm Update: N2 In 2025 (anandtech.com) 3nm Technology - Taiwan Semiconductor Manufacturing Company Limited (tsmc.com)

[5] Intel Demonstrates Breakthroughs in Next-Generation Transistor... Intel Accelerated

The increasing technical complexity calls for more efficient design and production methods. At factory level, solutions based on advanced mathematics, statistics or AI should enable extension across current domains enabling a wider scale integration. Advanced data modelling and analysis techniques, combined with generative AI should rapidly enable smarter detection of deviations (whether its process or product quality, equipment or global production performance) together with faster reaction thanks to AI augmented troubleshooting and guided analysis.

The intricate nature of future semiconductor manufacturing equipment requires a substantial increase in skilled labor for design and realization. Without advancements in efficiency, the local labor market may fall short in providing the necessary expertise, potentially slowing down innovation and affecting profit margins. In this domain as well, generative AI can be instrumental in mining existing knowledge deposits to support transfer to new generations. New methods will have to be developed to ensure the efficiency of this transfer and the sustainability of European know-how. While the use of generative AI should also enable the integration of this knowledge into software assistants or copilots and eventually autonomous systems, techniques will have to be developed to ensure that the system will stay in (human) control.

Automation trends like Industry 4.0 and 5.0 are reshaping manufacturing, demanding greater data exchange and secure integration of design data into production processes. This evolution aligns with the Smart Industry roadmap.

Environmental considerations are also at the forefront, with efforts to eliminate toxic substances such as PFAS-containing materials and SF6 gas from equipment and processes. Companies are committed to ambitious NetZero goals, focusing on enhancing energy, water, and material efficiency while exploring recycling opportunities for gases like hydrogen and carbon dioxide, as well as processed materials and consumables. Collaborations with equipment and materials suppliers are key to these initiatives, which include refurbishing and reusing components.

Overall, these developments pose significant challenges to the global semiconductor industry across various domains, but also present opportunities for European equipment vendors and their supplier networks.

The overarching goal of equipment development is to lead the world in miniaturisation techniques by providing appropriate products two years ahead of the shrink roadmap of the world's leading semiconductor device and components manufacturers[6]. Internationally developed roadmaps such as the International Roadmap for Devices and Systems (IRDS) will also be taken into consideration[7]. Currently, leading integrated device manufacturers (IDMs) are forecasting a continuation of the technology roadmap following Moore's law at least until 2029[8], which corresponds to at least four new generations after the current technology node.

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[6] https://investor.tsmc.com/english/encrypt/files/encrypt_file/qr/phase5_support/TSMC%201Q20%20transcript.pdf

[7] https://irds.ieee.org/

[8] https://www.anandtech.com/show/15217/ intels-manufacturing-roadmap-from-2019- to-2029

All-in-all, this represents a major challenge to the international semiconductor industry in the areas of lithography, material innovation, processing, assembly, process control, analysis and testing, as well as an opportunity for the well-positioned European equipment vendors and their network of suppliers.

1.1.3.4.3 Key focus areas

The key focus areas for innovative semiconductor manufacturing equipment technologies are as follows.

Topic 4.1 Wafer fabrication equipment

- Advanced patterning equipment for sub-2 nm node wafer processing using deep ultraviolet (DUV) and EUV lithography, and corresponding subsystems and infrastructure (e.g. pellicles, masks and resist).
- Mask manufacturing equipment for sub-2 nm node mask patterning and tuning, defect inspection and repair, metrology and cleaning.
- Advanced holistic lithography using DUV, EUV and next-generation lithography techniques, such as e-beam and mask-less lithography, directed self-assembly (DSA) and nano-imprinting.
- In-line wafer inspection and analysis for process control, defect detection, contaminant control etc.
- Multi-dimensional metrology (MDM) and inspection for sub-2 nm node devices that combine all the spectrum of physical tools and data processing techniques.
- Thin film processes including thin film and atomic layer deposition, doping and material modification, and corresponding equipment and materials, able to support the increase of binary, ternary and quaternary materials
- “Bottom up” technologies to selectively deposit materials on topography or on a selected material.
- Integrated surface preparation, deposition and etch process technologies for optimal interface engineering.
- Innovative equipment and process strategies for perfect gapfill of metals and dielectrics in decreasing feature sizes.
- Equipment and manufacturing technology for wet and dry processing, wet and dry etching, including (atomic layer) selective etch processing, thermal treatment, laser annealing and wafer preparation.
- Increased utilization of AI and modelling (e.g. computational chemistry) techniques for material and process development.

Topic 4.2: Wafer fab equipment for differentiated and/or mature technologies

- Technologies and tools for the manufacturing and integration of semiconductor components made with advanced nanomaterials and metamaterials (low-thermal-budget-processing 2D materials, nanowires, nanoparticles, quantum dots, etc) with logic and memory technologies.
- High-volume manufacturing tools for the production of III-V, GaN, SiC or other material substrates of up to 200 mm, or 300 mm in the future.
- Enable productivity enhancements (e.g. wafer diameter conversions) for heterogeneous integration technologies to significantly improve cost-competitiveness.

- New manufacturing techniques combining chip and packaging technologies (e.g. chip embedding), which will also require new manufacturing logistics and technologies (e.g. panel moulding).
- Dedicated equipment for manufacturing of electronics on flexible, structural and/or bio-compatible substrates.
- New electroplating equipment for ionic liquids (i.e. for Al deposition).

Topic 4.3: Automated manufacturing technologies including fab robotics and wafer transport & handling, required to enable IC-fabs with interconnected tools to support flexible, sustainable, agile and competitive high-volume semiconductor manufacturing[9]:

- Enable flexible line management for high-mix and distributed manufacturing lines, including lines for fabrication and deposition of advanced functional (nano) materials.
- Develop infrastructure technology to interconnect systems from various companies… And anticipate, configure, optimize, etc.
- Implement fast (and deep) learning as well as semi-automated AI-based decision-making to control processes, to enhance quality, increase reliability, shorten time to stable yield, preserve knowledge and master complexity.
- Apply Productivity Aware Design (PAD) approaches with a focus on predictive maintenance, virtual metrology, factory simulation and scheduling, wafer-handling automation and the digitisation of the value chain for AI-based decision management.
- Doubling semiconductor manufacturing in Europe in 2030 also means evolving and upgrading installed base through incremental approaches, which will necessarily mean increased complexity. Managing such hybrid factories will require advanced decision support and diagnosis techniques leveraging GenAI, Retrieval Augmented Generation (RAG) and integrating existing human knowledge and know how.
- Developing comprehensive modelling and sharing techniques, to enable seamless flow and utilization of information across the whole value chain, will require significant evolution of the existing knowledge management techniques and technologies (NLP to exploit existing documentation, diffusion and sharing of cutting-edge or strategic knowledge).

Topic 4.4: Sustainable semiconductor manufacturing

- Future innovations should also address new environmentally friendly solutions for manufacturing (e.g. in terms of energy consumption, chemical usage) and environmentally friendly new materials (e.g. in terms of quality, functionality, defects) in parallel with addressing the continued cost of ownership challenges. This will entail, for example, new precursors, chemicals for deposition and other wafer-processing materials, as well as gas delivery, gas handling, pumps and abatement systems. This will also comprise the study and implementation of new solutions for both effluent segregation as described above, including PFAs, as well as for recycling of water and other chemicals.

[9] 2023 IRDS Factory Integration (ieee.org)

Major Challenge 5: Advanced packaging, assembly & test equipment solutions

Semiconductor packaging and assembly equipment refers to the machinery and tools used in the process of packaging and assembling integrated circuits (ICs) and other microelectronic devices. Packaging is a crucial part of semiconductor manufacturing as it protects the semiconductor die, connects the chip to a board or other chips, and conducts heat dissipated by the components it contains. It affects power, performance, and cost on both macro and micro levels. The equipment includes various types of machinery from wafer dicing, encapsulation (or moulding) of the die into a plastic package, wire-bonding (on thermal compression, ultrasonic, and stitch bonding), wireless bonding (quasi-monolithic, hybrid bonding) to package marking and labelling equipment.

Semiconductor test equipment is used to evaluate the functionality and performance of semiconductor devices, such as integrated circuits (ICs), during and after the manufacturing process. This equipment is essential for ensuring that the devices meet the required specifications and quality standards before they are shipped to customers. The main types of semiconductor test equipment include Automatic Test Equipment (ATE), Wafer Test Equipment, In-Circuit Test (ICT) etc. These tools are crucial for detecting defects, ensuring reliability, and maintaining high yield rates in semiconductor manufacturing.

1.1.3.4.4 State of the art

The current state of the art in semiconductor packaging and assembly equipment is highly advanced and includes several key technologies that have emerged over the past two decades. Current advanced packaging technology uses sophisticated methods to aggregate components from various wafers, creating a single electronic device with superior performance. It is particularly important for applications like 5G, autonomous vehicles, IoT technologies, and virtual/augmented reality, which require high-performance, low-power chips capable of processing large amounts of data.[10] 3D Integration: Techniques such as 2.5D, 3D, fan-out, and system on-a-chip (SoC) packaging have been developed to supplement traditional wire-bonding and flip-chip technologies. These methods allow for higher density and performance by stacking chips vertically or integrating multiple chips into a single package. In the specific case of chiplets, the approach involves designing chips in a modular fashion that can be integrated with other types of chips to create a complete system. It allows for more flexibility in design and can lead to improvements in performance and power efficiency.

Yet, while reducing the complexity of design, 3D integration - when done at wide scale - should considerably complexify production and supply chain management. Integrating multiple chips in a single package will introduce a new level of complexity in assembly lines which will have to synchronize multiple flows, both internally (bring the right quantity and quality to the machine) and externally, i.e., at supply chain level, across various front-end facilities or even companies. Designing and operating robust supply chains will require digital twins operating at much wider scale.

The current state of the art in semiconductor test equipment is characterized by several key advancements. Machine Learning has been integrated into test systems to analyze large volumes of test data in real-time. This allows for the detection of subtle defects or performance deviations that might be

[10] https://www.mckinsey.com/industries/semiconductors/our-insights/advanced-chip-packaging-how-manufacturers-can-play-to-win

missed by traditional methods. Similarly, Machine Learning algorithms predict when automated test equipment (ATE) is likely to fail, enabling proactive maintenance to minimize downtime. With the rollout of 5G networks and the proliferation of IoT devices, test equipment providers have developed innovative solutions to meet the demands for higher data rates, lower power consumption, and greater reliability and availability.

These advancements in packaging and test equipment have helped ensure that semiconductor devices meet the necessary quality and performance standards. This is critical for the reliability and functionality of modern electronics. As the industry continues to evolve, we can expect further innovations in semiconductor packaging, assembly and test equipment to enhance performance, reduce costs, and improve reliability.

1.1.3.4.5 Vision and expected outcome

The future developments for semiconductor packaging and test equipment are expected to focus on several key areas which may reshape the industry. [11]

As devices become smaller and more complex, advanced packaging technologies like system in-package (SiP) and 3D stacking are becoming important. The advanced multichip packaging approach integrates multiple semiconductor components into a single package, which is well-suited for applications such as mobile devices, automotive computing, and generative artificial intelligence (GenAI). It aims to improve performance and time-to-market while reducing manufacturing costs and power consumption. High-Density Fan-Out, 2.5D IC, and 3D IC Packaging Technologies are becoming increasingly crucial for future data-centric applications. To maximize the benefits from ICs fabricated in nodes of 7 nm and below, the equipment will need to enable complex 3D structures with Through Silicon Vertical Interconnect Accesses (“TSVIA”), micro-bumps and thin dies, as well as wafer-to-wafer bonding, to speed up production of 3D ICs.

Packaging equipment must be modified to meet the decreasing feature sizes and increasing precision requirements of advanced packaging. This may lead to the introduction of packaging equipment in the front-end part of semiconductor manufacturing and, hence, increased requirements to contamination control.

Further equipment developments include functional diversification of technologies, where digital electronics meet the analog world, using advanced assembly/packaging of heterogeneous pieces of chips (“chiplets”) and of chips, sensors and/or smart antenna components. It should be noted that these trends are closely related to the trends formulated for (front-end) wafer-fab equipment, amongst others creation of silicon vias and backside power distribution networks.

An ongoing focus on enhancing functionalities of heterogenous systems by combining “traditional” semiconductors with iphotonics components or chiplets and addressing high speed component transfer by the assembly industry, with ambitious goals of developing transfer capability up to 1 million components per hour (without physical manipulation) by 2028.

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[11] https://www.bcg.com/publications/2024/advanced-packaging-is-reshaping-the-chip-industry

Besides this technological frontier, other trends for assembly equipment will also play a role. For example, factory automation to increase product reliability with multi-facetted device inspections, sorting and advanced tracking and tracing as well as data storage throughout the whole of the

production lines; product developments for highly specialized applications such as power modules, medical applications, organ on chip devices, communication and agrifood; development and application of 3D printing technology in heterogeneous integration, covering materials, process and equipment.

The future developments for semiconductor test & inspection equipment are anticipated to be influenced by several emerging trends and technological advancements. Building on the existing state of the art, further integration of AI and Machine Learning will play a significant role in transforming test engineering and the connected equipment. They will enable real-time analysis of extensive test data, identify subtle defects, and optimize test patterns to reduce test durations and enhance efficiency. As devices become smaller and more complex, new testing strategies and specialized test fixtures will be developed to access intricate device connections and ensure quality and performance in advanced packaging technologies. Test equipment designers will also need to explore and integrate innovative approaches to enable improved wafer-level testing & inspection to catch defects early in the manufacturing process, which is crucial for maintaining high standards of quality.

These advancements by the EU high-tech equipment industry will help ensure that semiconductor devices meet the necessary quality and performance standards, which is critical for the reliability and functionality of modern electronics.

1.1.3.4.6 Key focus areas

Topic 5.1: Packaging & assembly equipment:

- Equipment and manufacturing technology supporting 3D integration and interconnect capabilities such as chip-to-wafer stacking, fan-out WLP, multi-die packaging, “2.5D” interposers, wafer-to-wafer sequential processing, TSVs and transistor stacking.
- Enhanced equipment optimised for high-volume manufacturing of large batches of the same package and efficient reconfigurable equipment for the manufacturing of different packages in smaller batches.
- New process tools for die separation, attachment, thinning, handling and encapsulation for reliable heterogeneous integration on chip and in package, as well as assembly and packaging of electronics on flexible substrates.
- Equipment development to suit the requirements of multi-component assembly on flexible and stretchable substrates, especially in roll-to-roll for both conductive adhesives and soldering.
- New selective bonding equipment based on inductive or reactive heating.
- Equipment solutions for handling glass substrates and enabling Through Glass Via’s and glass plating.

Topic 5.2: Test and inspection equipment:

- In-line and off-line technologies for the Testing, Validation and Verification (TV&V) of heterogeneous chips and SiP with ever-increasing number of features and ever-decreasing feature size to tackle the challenge of failure localisation in these highly complex (packaged) chips.
- Characterisation and inspection equipment for quality control at multiple levels and different scales of semiconductor structures, films and components.

1.1.1.1 Major Challenge 6: Sustainability of semiconductor manufacturing

The semiconductor industry is living a paradox. On the one hand, continuous advances in chip capabilities are propelling the global effort to reduce carbon emissions through electrification and energy efficiency improvements in devices and all types of equipment. On the other hand, semiconductor manufacturing causes significant emissions itself, responsible for large CO_2 and Green House Gas (GHG) outputs. As an example, the carbon footprint of ICT was evaluated at about 1200–2200 $MtCO_2$ eq. in 2020, or equivalently 2.1%–3.9% of the world greenhouse gas (GHG) emissions. A significant part of this footprint, i.e., between 360 and 660 $MtCO_2$ eq., is attributed to the semiconductor-manufacturing phase[12].

At the same time, the semiconductor manufacturing industry must answer to the unprecedented demand for semiconductors across the industry for big emerging technologies such as AI/ML, Gen. AI, IoT, EVs and 5G/6G networks. This demand may double in the next four to six years. Therefore, reducing the CO_2 and GHG emission in semiconductor manufacturing is of utmost importance for the semiconductor industry.

In addition, or coupled to CO_2 and GHG emission, semiconductor manufacturing is resource intensive in energy, water, chemicals and raw materials. Moreover, the use of energy, water and other resources by the semiconductor industry continues to increase as wafer processing becomes more complex and as the industry expands production worldwide.

Furthermore, the semiconductor industry uses PFAs-containing materials in numerous critical applications. They are primarily utilized in the photolithography process to facilitate the smooth transfer of patterns onto the semiconductor substrate. PFAs stands for per- and poly-fluoroalkyl substances, known as “forever chemicals” (PFAs have lifetimes in the thousands of years), and refers to synthetic chemical compounds that contain multiple fluorine atoms attached to an alkyl chain. The broad definition of PFAs by the Organization of Economic Cooperation and Development encompasses more than 10,000 unique chemicals. Because of human health and environmental factors associated with the persistence, bioaccumulation and toxicity of several PFAs, legislative and regulatory efforts worldwide are seeking to initiate restrictions that could limit the use of PFAs-containing materials.

[12] T. Pirson et al. 2023, “The Environmental Footprint of IC Production: Review, Analysis, and Lessons From Historical Trends”, IEEE Trans. on Semicon. Manuf. 36, 1, 56-67

1.1.1.1.1 State of the art

For decades, the ECS community spent many efforts for enhancing the energy efficiency of electronic components for computing and sensing thanks to aggressive improvements to circuit design, component integration, and software, as well as power-management schemes and integration of specialized accelerators. However, the flip side is that higher energy efficiency does not necessarily translate to lower CO_2 and GHG emissions from semiconductor manufacturing processing.

According to the GHG Protocol, there are three types of GHG emissions (Fig. 1):

- Scope 1 – direct emissions from business operations and manufacturing.
- Scope 2 – indirect emissions, including those from power plants, to meet business energy requirements
- Scope 3 – emissions including all other indirect emissions in a company's value chain; upstream emissions are those generated by suppliers or their products, while downstream emissions are related to the usage of products containing semiconductors during their lifetime. Scope 3 downstream emission is nearly independent of the semiconductor-manufacturing phase.

In a typical semiconductor fab, 35% of GHG emissions fall into the Scope 1 category, compared with 45% for Scope 2, and 20% for Scope 3 upstream[13].

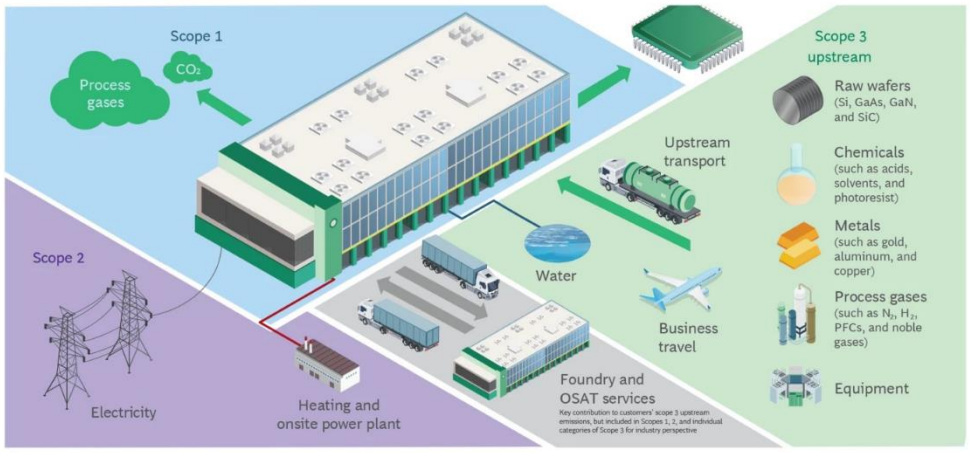

Figure 1: GHG emission sources from the semiconductor manufacturing

With about 80% of semiconductor manufacturing emissions falling into either scope 1 or scope 2 categories, semiconductor manufacturing lines control a large portion of their GHG emission profile. 85-90% of scope 1 emissions arise from fluorinated process gases used during wafer etching and cleaning, and chamber cleaning, while 10-15% originate from the use of fluorinated heat-transfer fluids. These

[13] "Keeping the semiconductor industry on the path to net zero", McKinsey & Company November 2022

gases, which include perfluorocarbons (PFCs), hydrofluorocarbons (HFCs), NF_3, SF_6 and N_20 have high global-warming potential (GWP) as well as a long atmospheric lifetime. Moreover, their emission rises as node size shrinks. According to the sixth assessment report of the Intergovernmental Panel on Climate Change, GWP100 values (defined as a relative GWP value for the period of 100 years with respect to CO_2) of CF_4, C_4F_8, NF_3 and SF_6 are 6630, 10200, 16100 and 23500, respectively.

To reduce PFC emissions, several strategies, such as alternatives, process optimization, recycling/recovery and abatement have been attempted.

The use of alternative materials to PFCs is expected to reduce PFC emissions by employing environmentally benign chemistries with low GWPs. However, finding relevant alternative materials will require significant R&D efforts. Process optimization through increasing the efficiency of PFC-consuming processes by adjusting process parameters, such as temperature and chamber pressure, can reduce PFC usage and, correspondingly, PFC emissions. Recycling/recovery and abatement of PFCs from exhaust streams can also control PFC emissions.

Scope 2 emissions, which represent the highest proportion of GHG from semiconductor companies, are linked to the energy required to run their extensive production facilities. The sources of these emissions include the following:

- Tool fleets containing hundreds of manufacturing tools, such as lithography equipment, ion implanters, and high-temperature furnaces. Their energy consumption represents the most part (39%) of a typical semiconductor fab[14].
- Large clean rooms requiring climate and humidity control with overpressure and particle filtration.
- Extensive sub-fab facilities for gas abatement, exhaust pumps, water chillers, and water purification.

As the node size of chips continues to shrink, energy requirements at production facilities are expected to rise significantly. Indeed, the energy consumption for manufacturing of a 28nm and a 3nm 300mm wafer has been modelled to be 400 and 1400 kWh, respectively[15]. The facility energy was not included in this model.

Lowering greenhouse gas emissions is one of the semiconductor industry's most complicated challenges due to the energy needed to make chips and the unique requirements of the manufacturing processes. This complexity is even enhanced as the semiconductor industry must also expand globally to meet the growing demand for chips.

Semiconductor manufacturing is also extremely-water intensive and requires large volumes of ultra-pure water to avoid the contamination of electronic devices. A typical semiconductor manufacturing facility uses 7.5 to 15 million litres of ultra-pure water per day, and it takes about 6,000 litres of city water to create 3,800 litres of ultrapure water. In response to prolonged droughts and increasing demand for

[14] S-C. Hu et al. 2020, "Energy savings approaches for high-tech manufacturing factories", Case Studies in Thermal Engineering 17, 100569

[15] M. Garcia Bardon et al., "DTCO including Sustainability: Power-Performance-Area-Cost-Environmental score (PPACE) Analysis for Logic Technologies," 2020 IEDM, San Francisco, CA, USA, 2020,

semiconductors, the semiconductor industry is focusing on new ways to recycle, reduce, and reuse the water used in their production. New advancements in water treatment have emerged to allow semiconductor manufacturers to recover and reuse wastewater and remove targeted contaminants. They allow reaching a water recycling rate, defined as the ratio between the recycled water and the total water use (which is the sum of recycled water use and water intake)-, ranging from 12 to 70%[16]. However, since the demand for semiconductors will strongly grow in the coming years, the semiconductor industry must improve its recycling water rate, especially in water-stressed countries.

Given its carbon-fluorine chemistry, PFAs-containing materials offer a unique set of surface tension, stability and chemical compatibility that many semiconductor applications require. The following paragraphs highlight key uses and challenges of PFAs in each of the application groupings, which are critical to the semiconductor industry:

- **Photolithography** materials containing PFAs are a critical component used within photoacid generators in chemically amplified resists and bottom antireflective coatings, top antireflective coatings, surfactants, barrier layers, photo-imageable polybenzoxazoles and polyimides for dielectric and buffer coat applications, and photoresist applications. The amount of PFAs consumed in each technology node depends on the number of masks used and the complexity of the multipatterning steps.
- **Wet chemistries** are applied within semiconductor manufacturing for cleaning, stripping, wet etching, chemical mechanical planarization, metal plating, and to facilitate other processes. Most wet chemistry applications do not contain PFAS. However, there are some applications that rely on PFAs materials for specific performance requirements. Examples of these applications include - but are not limited to - post-plasma photoresist strip, high aspect ratio collapse mitigation, selective film inhibition, wetting of low surface energy substrates, and specific parts cleaning.
- **Dry etching and deposition process**: Perfluorocarbons (PFCs) and hydrofluorocarbons (HFCs) are essential gases for directional etching and cleaning of silicon compounds. Additionally, fluorinated organometallic compounds are essential for the deposition of metal-containing films. Some PFCs and HFCs are part of the PFAs category such as CF_4, C_2F_6, C_4F_8 and C_3F_8.
- **Heat Transfer Fluids** (HTFs): Many semiconductor-manufacturing processes entail physical and chemical processes that require precisely controlled temperatures, and thus are highly reliant on HTFs. In both cooling and heating applications, fluorinated HTFs (F-HTFs) help ensure the ability to provide the precise temperature control required in specific manufacturing operations within the semiconductor fabrication process.
- **Semiconductor manufacturing and related equipment** and infrastructure articles. Semiconductor manufacturing facilities and the manufacturing equipment and infrastructure within them contain a multitude of articles. An article is any object made from one or more substances and mixtures which during production is given a special shape, surface or design that determines its function to a greater degree than its chemical composition, whether on its own or in an assembly with other articles, substances and mixtures. PFAs-containing articles include those made of a fluoropolymer, articles coated or painted with a fluoropolymer, or other PFAs-containing materials (such as oligomers) and those made of non-PFAs polymers containing PFAs

[16] Wang Q. et al. 2023, “Water strategies and practices for sustainable development in the semiconductor industry”, Water Cycle 4, 12–16

processing/machining aids or additives. Many semiconductor manufacturing applications require the use of PFAs-containing articles for safety, contamination control, resilience and other factors.

- **Pump fluids and lubricants**. Semiconductor manufacturing relies on the extensive use of robotics, automation and vacuum systems to achieve nanometre-scale precision. The use of lubricants, many of which need to be fluorinated, is essential to the precision and reliability of these systems.

Due to the extremely wide range of individual PFAs and their respective use cases in the semiconductor manufacturing process, time frames for finding and deploying alternatives can be very long, even in best-case scenarios. Depending on the use case, an alternative that has the same functionalities must first be invented and tools and/or process facilities must be adapted before said alternative could be qualified and deployed. As an example, some alternatives are currently developed for substituting PFAs in HTFs, in working fluids for vacuum pumps and in some articles in equipment. However, no alternatives to PFAs are available in photoresists, developers, antireflective coatings, rinsing solutions, wet and dry etching[17].

The short-term approach to reduce or even prevent the emission of PFAs from the semiconductor industry is to remove PFAS-containing materials from fab water, solvent wastes, gases and chemical vapours.

1.1.1.1.2 Vision and expected outcome

Since GHG emissions from a typical semiconductor fab arise from its power/energy consumption, identifying strategies for reducing power consumption in a semiconductor manufacturing line looks mandatory. Process optimization is one approach to reduce the energy consumption. It requires a close collaboration between chip manufacturers, R&D labs and tool suppliers by simultaneously optimizing yield and energy consumption during the least energy-efficient process steps. Similarly, such collaborations should also help equipment suppliers to manufacture more energy-efficient equipment and materials.

As the energy and water consumptions of a typical semiconductor manufacturing line depend on the number of process steps, and evolve proportionally[18], reducing the energy consumption through process optimization should also lower the water consumption. However, the most convenient approach to lower the water intake of the semiconductor industry, is to enhance the current water recycling rate in order to reach a rate higher than 70% in the coming years.

Finding alternative gases for replacing PFCs will be long and costly, because only few green solutions are now viable alternatives to current gases. It seems to be easier to find alternatives for fluorinated gases for cleaning processes (pre-clean, seasoning, chamber cleans) than for dry etching. Looking for such viable alternatives will require narrow collaboration along the semiconductor supply chain from R&D labs and chemical suppliers to the semiconductor manufacturers.

Hence, over the short to mid-term, the current solution to decrease GHG emissions from fluorinated gas usage is the implementation of abatement systems to contain and decompose the problematic

[17] Lay D. et al., "A guide to PFAS in electronics", ChemSec H2020 Project No. SA22171340

[18] Wang Q. et al. 2023, "Environmental data and facts in the semiconductor manufacturing industry: An unexpected high water and energy consumption situation", Water Cycle 4, 47–54

compounds. The current abatement efficiency in a semiconductor manufacturing line typically ranges from 20 to 65%[19]. This abatement rate should be enhanced in a short term. This will remain the case until alternative gases with fewer emissions are available, or until gas recycling is widely adopted.

Gas recycling is another approach for reducing GHG emission from the semiconductor industry. It consists in capturing unutilized process gases and by-products through various means, such as membrane separation, cryogenic recovery, adsorption, and desorption. They can then refine them into pure process gases that can be used again, potentially reducing process-gas emissions. For this lever to become economically viable, researchers will need to address major challenges related to the separation of process-gas outflows and purification.

Concerning PFAs, the semiconductor industry recognizes the need for, and is undertaking additional R&D to:

- Characterize the human health and environmental risks associated with PFAS-containing materials used in the industry.
- Develop analytical methods to characterize PFAS-containing materials.
- Evaluate PFAS releases to air and/or water.
- Identify, test and implement substitutes to either eliminate PFAS-containing materials, or substitute PFAS-containing materials with those having lower human health or environmental risks.
- Evaluate and test abatement technologies to capture or destroy PFAS-containing materials before their release to the environment.

1.1.1.1.3 Key focus areas

Topic 6.1: Semiconductor manufacturing line:

- Enhanced water recycling rate including the full removal of PFAs from wastewater.
- Enhanced efficiency of gas abatement systems for reducing GHG and PFAs emissions in the atmosphere.
- Optimized process steps for reducing the energy consumption of the least energy-efficient steps, while maintaining high manufacturing yield.

Topic 6.2: Equipment and material suppliers:

- Improve energy efficiency of the equipment.
- Implement re-use of parts/modules for equipment maintenance and servicing.
- Reduce the use of PFAs-based materials in equipment production.
- Find viable alternatives to PFAs for etching and layer deposition.
- Find alternatives to PFAs for photolithography resists and wet chemistries.

[19] S. Jones “IEDM 2023 – Modeling 300mm Wafer Fab Carbon Emissions”, https://semiwiki.com/semiconductor-services/techinsights/340325-iedm-2023-modeling-300mm-wafer-fab-carbon-emissions

1.1.4 Timeline

All leading European industry and research actors should align their activities with international roadmaps and timelines. Roadmap exercises are being conducted in various projects and communities, including NEREID[20] and the IEEE's IRDS[21], in which European academia, RTOs and industry are participating. For system integration, the International Electronics Manufacturing Initiative (iNEMI)[22] and the new Heterogeneous Integration Roadmap activities are also considered. The European R&D priorities are planned in synchronisation with global timeframes and developments that are under continuous adaptation. The timelines below are high-level derivatives from these global evolutions, and follow the structure of the four Major Challenges described above.

For Major Challenge 1, the roadmap for process technology and device/system integration presents relatively clear timelines, although economic factors will determine the speed of adoption in industrial manufacturing. Dedicated process technologies (e.g. low-power and high-operating temperature) will follow feature scaling with some delay, focusing on other performance indicators. Areas where the roadmaps and timelines are less clear (e.g. new computing paradigms) will be introduced at low technology readiness levels (TRLs).

For Major Challenges 2 and 3, the timeline of the implementation of new technologies largely depends on the needs and roadmaps of the systems, and will result from the interaction within application-driven projects and test-bed initiatives. The timing of new equipment and manufacturing solutions for these challenges should be derived from the schedules of the major European semiconductor manufacturers. This includes roadmaps for key future semiconductor domains, such as automotive, healthcare, safety and security, power, MEMS, image sensors, biochips, organ-on-a-chip, photonics, lighting, etc. Fast implementation and modification of these new device technologies will pave the way for the technologies of tomorrow.

First, the development of sub-2nm solutions in terms of equipment and materials as part of Major Challenge 4 needs to be two-to-three years ahead of mass adoption, and is of critical importance to maintaining European leadership. Second, new equipment and materials solutions should be developed in line with the needs defined in the roadmaps of Major Challenges 1–3. Lastly, improving manufacturing efficiency and enhancing yield and reliability are ongoing tasks that need to be performed in accordance with the needs of the "More-Moore" and "More-than-Moore" domains. Fundamentals of "manufacturing science" will concern projects at rather low TRLs (typically 3–5), whereas implementation in pilot lines and full-scale production lines will contemplate higher TRL projects (typically 7–8). For most of the manufacturing science projects, the execution will take place in the medium- to long-term timespan, although the shorter-term impact, such as improving the uptime of equipment due to Productivity Aware Design or the improvement of robustness of the manufacturing processes, will get due attention to enhance competitiveness.

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[20] https://www.nereid-h2020.eu/
[21] https://irds.ieee.org/
[22] https://www.inemi.org/ https://eps.ieee.org/technology/ heterogeneous-integration-roadmap/2019-edition.html

Major challenge	Topic	Short term (2025 – 2029)	Mid term (2030-2034)	Long term (2035 and beyond)
Major challenge 1: Advanced computing, in-memory, neuromorphic, photonic and quantum computing concepts	**Topic 1.1:** Extensions of the scaled Si technology roadmaps High-performance Ultra-low power 3D integration	Sub-N2 R&D 2nd generation gate-all-around devices, forksheet integration 18 nm FDSOI at technology platform integration level	N1,5 R&D - 3rd generation of Gate-All-Around devices CFET introduction 12/10 nm FDSOI at technology platform integration level 3D monolithic integration	Sub-1 nm node logic and memory technology (nanowires, nanosheets) at process and device research level Vertically stacked nanosheets 3D monolithic integration Beyond 10 nm FDSOI at technology platform integration level
	Topic 1.2: Exploration and implementation of unconventional devices based on materials beyond Si	SiGe (high Ge) channel Cu alternative solutions	Ge channel Optical interconnects 2D materials exploration	III-V channel Low-thermal-budget-processing 2D materials device integration
	Topic 1.3: Novel device, circuit and systems concepts, such as for near/in-memory, neuromorphic, optical and quantum computing	Near/in-memory computing 3D heterogeneous integration (logic/memory)	In-memory computing Neuromorphic computing (spiking) 3D monolithic integration Photonic SOI	Quantum computing Optical computing
	Topic 1.4: Long-term challenges such as steep-slope switches, spin-based transistors and alternatives		TFET CNTFET 2D material FET	NCFET NEMS switch Topologic insulator electronic devices Spin wave devices Mott FET (VO2, HfO2, etc)
	Topic 1.5: New eNVM technologies	PCRAM STT-MRAM FDSOI embedded MRAM and/or PCRAM	PCRAM PCRAM (MLC) SOT-MRAM ReRAM FeRAM	ReRAM (MLC) Hi-density ReRAM TCRAM VCMA-MRAM ECRAM
Major challenge 2: Novel sensor, actuation and other devices that enable advanced functionality	**Topic 2.1:** Application-specific logic integration	ULP 18 nm FDSOI technology with embedded memory integration	12/10 nm FDSOI technology integration with memories New technology integration architectures for neuromorphic computing 3D monolithic or quasi monolithic stacking integration for heterogeneous elements	3D monolithic integration
	Topic 2.2: Advanced sensor and actuator technologies	Continuous improvement of sensitivity (imagers, IMU, etc), range (lidar), and reduction of individual sensor area and energy consumption Development of miniaturised low power chemical sensors Development of biomedical sensors integrated with micro/ nanofluidics Heterogeneous and quasi monolithic integration of sensor technologies with (ULP) logic/memory technologies, including 28/22 nm FDSOI for the IoT environmental protection technologies for audio MEMS	Quantum sensors (see 2.4) Ultra-low power chemical sensor systems for pollution monitoring Energy autonomous connected sensor systems Integrated biomedical sensor systems Heterogeneous and quasi monolithic integration of sensor technologies with novel device, circuit and systems memory and computing concepts, including 12nm FD-SOI for IoT Integrated technologies for enhanced robustness against environmental effects for MEMS based audio devices	Nanoelectronic sensor devices with individual molecule sensitivity and selectivity Nanoelectronic biomedical sensor systems Monolithic integration of sensor technologies with novel devices, circuit and systems memory and computing concepts 10 or Beyond 10 nm FDSOI for IoT

	Topic 2.3: Advanced power electronics technologies	Silicon, BCD, SiC and GaN-based technologies and substrate materials Energy-efficient systems, including energy harvesting	New CMOS and IGBT processes Smart GaN devices (combining logic and power devices) Vertical GaN power devices Towards 300 mm GaN and 200 mm SiC substrates Energy-autonomous systems Energy harvesting and energy storage systems	B-Ga_2O_3, AlN Diamond
	Topic 2.4: Quantum sensing technologies		Integration of cells used in trapped ions, neutral and cold atoms technologies, and entangled photons in a CMOS platform coupled to laser sources and (single) photon detectors Superconductor qubits Maintaining performance when manufactured at chip-scale and optimising SWaP-C (size, weight, power and cost).	Development of entangled qubits for improving the sensitivity growth of "large" diamond single crystals investigation of color centers-based qubits in wide bandgap semiconductors such as SiC, GaN
	Topic 2.5: Advanced RF and photonics communication technologies	Enable 5G connectivity RF and mm-wave integrated device options building on, for example, SiGe/BiCMOS (increase of ft), RF and FDSOI, CMOS, PIC,GaN/Si, GaN/SOI and GaN/SiC technologies Towards 300 mm GaN-Si substrates Next-generation SOI for mm-wave photonics SOI 200 mm POI	Improve RF front-End components roadmap (switches, LNA, antenna tuners) Strained materials Tiny silicon thickness and uniformity Improve linearity substrate behaviour RF substrate options for advanced CMOS nodes Integration of III-V semiconductors on silicon and SOI Integration of III-V semiconductors on photonics SOI RF interposer for heterogeneous integration combining III-V and CMOS 3D stacking of different functions (RF with digital, ...) New materials for advanced functions	
Major challenge 3: Advanced integration and solutions	**Topic 3.1:** Advanced interconnect technologies	Vertical as well as horizontal integration via TSV, TEV, microbumps Fan-out WLP or embedded wafer-level BGAs and chip- embedding in laminate materials Advanced wafer-stacking technologies Packaging & bonding technologies with advanced thermal management capability	3D stacking/horizontal connecting of dies/chiplets Advanced nanomaterials (including low-thermal-budget-processing 2D materials, nanowires, nanoparticles, etc) Critical raw materials elimination from packaging bill of materials such as W, Co, Mo, Be, BeO	
	Topic 3.2: Specific power, sensor and RF application technologies	RF component miniaturisation for mm-wave applications Package integration of additional functionality such as antennas, passive devices and power sources Challenges of optical packaging for recent optical sensors (Visible, NIR, IR)	RF miniaturisation for THz applications Packaging of wide bandgap materials (GaN, SiC, including specific challenges for higher power and voltage levels, etc) Optical packaging for PIC, lidars and for hyperspectral imaging applications	New cryogenic compatible packaging platforms for QIP Packaging solutions for extremely high power dissipation and new materials
	Topic 3.3: 3D integration technologies	Chip I/O-pad level 3D-SiC Chip-package-board co-design	3D SoC System technology co-optimisation 3D stacking for quasi-monolithic integration	Ultimate transistor-level 3D ICs ("monolithic" integration)

			(such as “sequential layering”)	
Major challenge 4: Advanced wafer fab equipment solutions	**Topic 4.1:** Wafer fabrication equipment	Manufacturing equipment for 2 nm node logic and memory Manufacturing equipment for 3D heterogeneous integration interconnect and interposer concepts down to 1 µm pitch	Manufacturing equipment for 1 nm node logic and memory Equipment to enable novel switches, transistors and alternatives based on, for example, 2D materials, topologic insulator and spin-wave devices Manufacturing equipment for 3D monolithic interconnect and interposer concepts below 1 µm pitch.	Manufacturing equipment for sub-1 nm node logic and memory Manufacturing equipment for sub-1 nm node transistor, 3D monolithic and optical interconnect concepts
	Topic 4.2: Wafer fabrication equipment for differentiated and/or mature technologies	Equipment for manufacturing of components with advanced nanomaterials Production tools for III-V, GaN, SiC or other material substrates of various thickness Production and metrology tools for wafer processing and alignment on opaque wafer substrates	Equipment for materials and processes for new eNVM types such as (high-density) ReRAM Production tools for 300mm for III-V, GaN, SiC or other material substrates of various thickness	
	Topic 4.3: Automated manufacturing technologies	Semantic integration of data for the modelling of finer process interactions over wider fabrication domains AI/ML enhanced systems Smarter detection of potential deviations and faster reaction through AI augmented insight and diagnostics Integrated Supply Chain to optimize production flows and resources utilization.	Autonomous solutions for factory operation (smart control rooms) with >90% of the deviations treated autonomously by the system. Automatic identification and allocation of tasks to responsible “agents” (whether human, robotic or software).	Quantum computing, semantic modelling and ubiquitous connectivity enable next level digital twins to operate 3D SoC ecosystems.
Major challenge 5: Advanced packaging, assembly and test equipment solutions	**Topic 5.1:** Packaging and Assembly equipment	Packaging & assembly equipment for chip-to-wafer stacking, fan- out WLP, multi-die packaging, “2.5D” interposers and TSVs 300 mm photonic SOI 200 mm POI	Packaging & assembly equipment to enable next-generation autonomous sensors, power electronics and RF/optical communication packaged ICs	
	Topic 5.2: Test and inspection equipment	Test & inspection equipment for chip-to-wafer stacking, fan- out WLP, multi-die packaging, “2.5D” interposers and TSVs.	Test & inspection equipment to enable next-generation autonomous sensors, power electronics and RF/optical communication packaged ICs	
Major challenge 6: Sustainability of semiconductor manufacturing	**Topic 6.1:** Semiconductor manufacturing line	Reduction of CO_2 and GHG emission and of the electrical consumption of semiconductor production lines Use of recycled and reclaimed water	Reduction of CO_2 and GHG emission from semiconductor production lines through better abatement systems and reduction of gas usage and leakage Use of 100% renewable energy sources	No CO_2 and GHG emission by replacing current GHG-related gases (NF_3, PFC…) by alternative chemistries Use of recycled metals to prevent the scarcity of some mineral ores Use of 100% recycled and reclaimed water
	Topic 6.2: Equipment and material suppliers	Improve energy efficiency of semiconductor equipment	Implement re-use of parts/modules for equipment maintenance and servicing Reduce the use of hazardous materials	